USN | | | | | | | | | | |

10ES32

Third Semester B.E. Degree Examination, Aug./Sept.2020
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Define DC and AC resistance of a diode. Determine V_0 for the circuit shown in Fig.Q.1(a). Assume diode is ideal. **(07 Marks)**

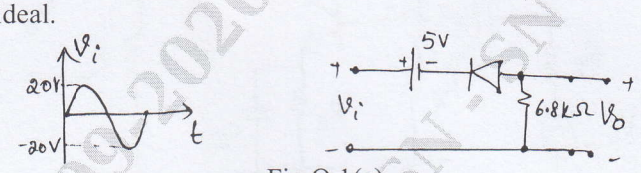

Fig.Q.1(a)

b. For the circuit shown in Fig.Q.1(b), obtain the output voltage $V_0(t)$ waveform and transfer characteristic plot for the input $V_i(t) = 30\sin wt$. Assume diodes are ideal. **(08 Marks)**

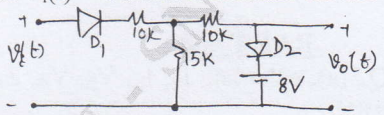

Fig.Q.1(b)

c. Explain the operation of a positive clamper. **(05 Marks)**

2 a. For the Voltage-Divider bias configuration shown in Fig.Q.2(a). Determine I_B, I_C, V_{CE}, V_C, V_E and V_B. Assume $\beta = 80$ and $V_{BE} = 0.7V$. **(07 Marks)**

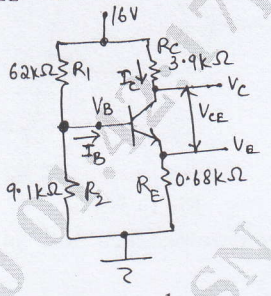

Fig.Q.2(a)

b. Design an Emitter stabilized network at $I_C = \frac{1}{2} I_{Csat}$ and $V_{CEQ} = \frac{1}{2} V_{CC}$. Use $V_{CC} = 20V$, $I_{Csat} = 10mA$, $\beta = 120$ and $R_C = 4R_E$. Assume $V_{BE} = 0.7V$ **(07 Marks)**

c. Derive the expressions for $S(I_{CO})$, $S(V_{BE})$ and $S(\beta)$ for the fixed bias BJT configuration. **(06 Marks)**

3 a. Derive the expressions for Z_i, Z_o and A_v for the voltage divider bias BJT configuration using r_e equivalent model. **(08 Marks)**

b. Write the Hybrid equivalent model of common base configuration (for pnp transistor). **(05 Marks)**

c. For the circuit shown in Fig.Q.3(c), determine r_e, Z_i, Z_o and A_v. Assume $\beta = 110$ and $V_{BE} = 0.7V_e$. **(07 Marks)**

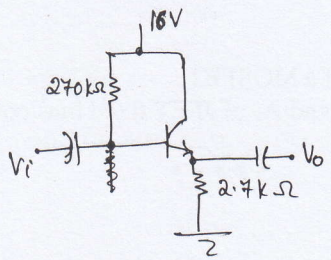

Fig.Q.3(c)

4 a. Derive the expression for the miller input capacitance and output capacitance. **(10 Marks)**

b. Determine the lower cutoff frequency for the circuit shown in Fig.Q.4(b) using low frequency response analysis for the following parameters $C_S = 10\mu F$, $C_E = 20\mu F$, $C_C = 1\mu F$, $R_S = 1K\Omega$, $R_1 = 40K\Omega$, $R_2 = 10K\Omega$, $R_E = 2K\Omega$, $R_C = 4K\Omega$, $R_L = 2.2K\Omega$, $\beta = 100$, $r_0 = \infty$ and $V_{CC} = 20V$. **(10 Marks)**

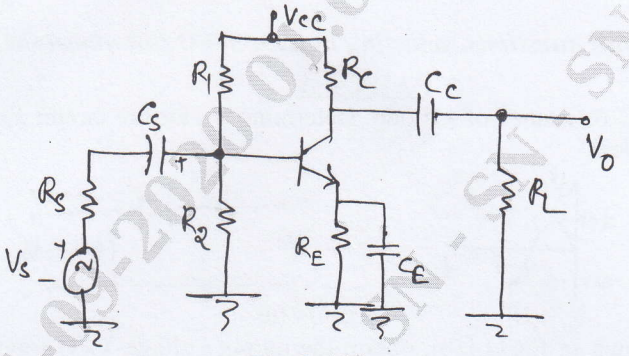

Fig.Q.4(b)

PART – B

5 a. For the circuit shown in Fig.Q.5(a), calculate I_B, I_E, V_E, V_B, Z_i and Z_o. Assume $\beta_D = 8000$, $V_{BE} = 1.6V$, $r_i = 5K\Omega$, $V_{CC} = 18V$. **(10 Marks)**

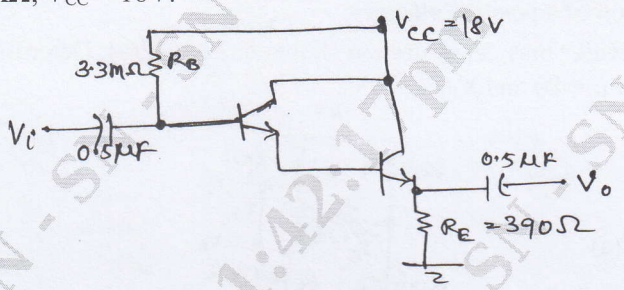

Fig.Q.5(a)

b. Derive the expressions for the input impedance and output impedance of voltage-shunt feedback amplifier. **(10 Marks)**

6 a. For class B amplifier providing a 22V peak signal to a 8Ω load and a power supply of $V_{CC} = 25V$. Determine the input power, output power, circuit efficiency, maximum input power and maximum output power. **(10 Marks)**

b. Explain the working of series-fed class A amplifier and prove that the maximum efficiency is 25%. **(10 Marks)**

7 a. Write the circuit diagram of Wein Bridge Oscillator circuit and explain. Write the expression for frequency of oscillation. **(10 Marks)**

b. Explain BJT crystal controlled operating in parallel resonant mode. **(05 Marks)**

c. In a transistor Colpitts oscillator find the value of L for a frequency of 110kHz. Assume $C_1 = 2nF$ and $C_2 = 80nF$. **(05 Marks)**

8 a. Obtain the small signal model of a MOSFET. **(10 Marks)**

b. Obtain the expression for Z_i, Z_o and A_v of JFET fixed bias configuration. **(10 Marks)**

* * * * *